Asymmetric Multi Processing (AMP) Linux + Bare-Metal on Altera SoC



Linux + Hard Real-Time (20 µs Cycle) on Dual Core ARM Cortex A9

Having two operating systems on the two ARM cores in an Altera Cyclone V or Stratix 10 SoC combines best of both worlds:

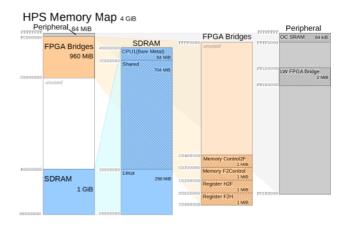


- CPU0: Linux Start-up, Communication, ...
 - · Standard OS with well known features
 - Kernel 4.1.22-ltsi-altera
 - Ångström-Distribution, Version v2015.12
 - Plenty of software available
 - Easy development of custom software
 - Easy firmware update (including bare-metal and FPGA) via SFTP etc.
- CPU1: Bare-Metal Control
 - Maximum speed
 - Cycle times down to less than 20 μs
 - No interrupts from Linux

This all is combined with an FPGA for programming custom "Hardware". That's maximum freedom on a single chip: the optimal environment for each type of requirements.

Features:

- Static memory map to divide between Linux, bare metal and shared memory
- No sharing of peripherals for maximum independence of systems¹
- No interrupts on bare metal for maximum predictability¹
- FPGA lightweight bridge for Linux, full bridges for bare metal



Software development and debugging for both cores with standard Altera SoC EDS. Separate or combined Debugging possible.

¹ Shared L2 cache and DDR memory of the dual core processor cause inevitable memory timing interferences between the cores, independent of the operating systems.